REMARKS

Claims 1-20 are pending in the application.

Claims 14-20 stand withdrawn as non-elected and are hereby cancelled without prejudice for presentation in a divisional application.

Claims 1-13 are rejected.

The drawings filed on January 2, 2004 are objected to by the Examiner.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5).

Claims 1, 4, 8 and 11 are rejected under 35 U.S.C. 102(e).

Claims 2-3, 5-7, 9-10 and 12-13 are rejected under 35 U.S.C. 103(a).

Claim 1 stands amended. Claims 21-26 are added.

No new matter is added.

Claims 1-13 and 21-26 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Notice of Non-Compliant Amendment – 37 CFR 1.121

Applicant submits this amendment in order to include marking changes in the Specification on page 2 of this amendment, in response to the Notice of Non-Compliant Amendment dated August 12, 2005.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference characters not mentioned in the description: 821 and 838 of FIG. 3, 151-152, 167, 171, 175, 183 of FIG. 4.

The specification has been amended to properly identify the reference characters in FIGS. 3 and 4.

The drawings are objected to because in FIG. 4 the character '111' should be showing the IC and not the substrate.

FIG. 4 has been amended to correctly connect the reference character '111' to the IC and not the substrate. The amended replacement sheet is enclosed in the Appendix following page 11 of this paper.

Claim Rejections - 35 USC § 102

Claims 1, 4, 8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pub 2002/0124518 to Karnezos.

Applicant respectfully traverses the rejections.

With respect to amended independent claim 1, the claim is amended to clarify that the electrical circuits on the lower surface of the substrate of the upper chip scale package are electrically connected to the electrical circuits on the lower surface of the substrate of the lower chip scale package. As shown in FIG. 4, the electrical circuits 165 of the upper chip scale package 150 are on the lower surface of the substrate 161 which is the same surface as the ball land pads 163. The electrical circuits 125 of the lower chip scale package 110 are on the lower surface of the substrate 121 which is the same surface as the ball land pads 123. The circuits 165 are connected to the circuits 125.

Karnezos, at FIG. 5A (and throughout FIGS. 5-11) discloses electrically connecting lower metal layer 523 of the top package 500 to the upper metal layer 421 of the bottom package 400. From the context of the present application, the electrical connection in Karnezos is from the lower surface of the substrate of the upper chip to the *upper* surface of the substrate of the lower chip. Thus, Karnezos does not disclose each and every element of independent claim 1.

Therefore, claim 1 is believed to be allowable over Karnezos and allowance is respectfully requested.

Claims 4, 8 and 11 all depend from independent claim 1, and for at least the reasons given for claim 1, these claims are believed to be allowable over Karnezos.

Claim Rejections - 35 USC § 103

Claims 2-3, 5-7, 9-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0124518 to Karnezos in view of US Pub 2004/0150107 to Cha, et al.

Applicant respectfully traverses the rejections.

Claims 2-3, 5-7, 9-10 and 12-13 all depend from independent claim 1 and, thus, necessarily include all of the elements of claim 1. With respect to claim 1, the addition of Cha does not cure the deficiencies of Karnezos. The combination of Karnezos and Cha still fails to disclose electrically connecting circuit patterns on the lower surface of the substrate of the upper stacked chip scale package to circuit patterns on the lower surface of the substrate of the lower stacked chip scale package. Thus, the combination of Karnezos and Cha fails to

disclose each and every element of independent claim 1. Because claim 2-3, 5-7, 9-10 and 12-13 all depend from claim 1, the combination also fails to disclose each and every element of these claims.

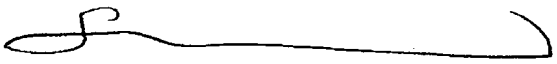
Thus, claims 2-3, 5-7, 9-10 and 12-13 are believed to be allowable over the combination of Karnezos and Cha and allowance is respectfully requested.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-13 and 21-26 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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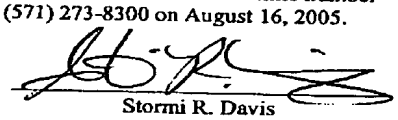
I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on August 16, 2005.



Stormi R. Davis

AMENDMENTS TO THE DRAWINGS

FIG. 4 is amended to correctly connect reference number 111 to the lower semiconductor chip. An annotated sheet showing changes and replacement sheet are enclosed in the Appendix following page 10 of this paper.

Dong-Ho LEE
STACK PACKAGE MADE OF CHIP SCALE PACKAGES
Attorney Docket No. 9903-074/Application No. 10/750,979

Annotated Sheet Showing Changes

1/1

FIG. 3

(Prior Art)

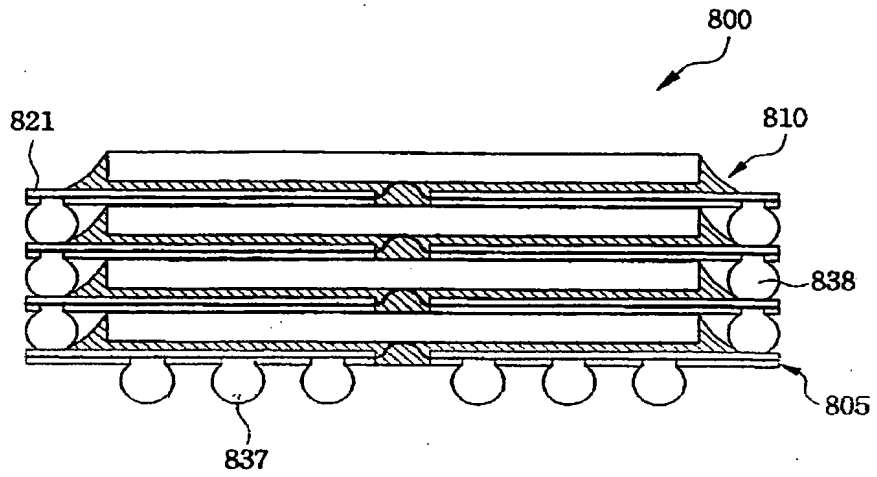


FIG. 4